UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,438	02/21/2002	Thomas E. Pearson	42390P13560	8225

7590 04/09/2003

Blakely, Sokoloff, Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER
VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,438	PEARSON ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-51* is/are pending in the application.

4a) Of the above claim(s) *33-39 and 44-49* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,10,12,13,16,18-20,23-28,40-42,50 and 51* is/are rejected.

7)☒ Claim(s) *4,5,9,14,15,17,21,22,29-32 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-10, 12-32, 40-43, 50 and 51, drawn to a package interposer, classified in class 361, subclass 768.

   II. Claims 33-39 and 44-49, drawn to process for making said interposer, classified in class 29, subclass 846.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and Claims 1-10, 12-22, 26-32, 40-43, 50 and 51 of Invention I are related as process of making and process of using the product. The use as claimed cannot be practiced with a materially different product. Since the product is not allowable, restriction is proper between said method of making and method of using. The product claim will be examined along with the elected invention (MPEP § 806.05(i)).

3. Inventions II and Claims 1-10, 12-22, 26-32, 40-43, 50 and 51 of Invention I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process wherein, instead of the coating step, only the amount of material required for the traces need be deposited.

4. Inventions II and Claims 23-25 of Invention I are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, Inventions II and Claims 23-25 have separate utility such as a process of making an interposer board (Invention II) and a process of coupling elements of an electronic package to a circuit board (Claims 23-25 of Invention I). See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

7. During a telephone conversation with Applicant's Attorney, Jordan M. Becker, on April 03, 2003 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-10, 12-32, 40-43, 50 and 51. **Affirmation of this election must be made by Applicant in replying to this Office action**. Claims 33-39 and 44-49 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

8. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

9. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

10. Claim 23 is objected to because of the following informalities:

Line 8 recites "the interposer such that...." Some text is missing between "interposer" and "such." For example, one possible correction could be the word --wired-- inserted after "interposer" in line 8 to make definite the limitation recited in lines 8-9.

Appropriate correction is required.

Rejections Based On Prior Art

11. The following references were relied upon for the rejections hereinbelow:

Olzak et al. (2002/0093803 A1) Higashiguchi et al. (US 5,760,469)

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1-3, 6-8, 10, 12, 13, 18-20, 23-28, 50 and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Olzak et al.

As to Claim 1, Olzak et al. discloses and apparatus comprising: a die, hidden by the PLCC encapsulation and a package (PLCC) coupled to the die (Fig. 3; p.1: paragraph [0007]); an interposer 100 (Fig. 2), fixedly coupled to the PLCC (Fig. 3) and formed from a circuit board substrate 102 (p.3: paragraph [0028]), by which the apparatus is electrically coupled to a circuit board (parent PWB; Fig. 3); interposer 100 has a first plurality of contacts 104 spaced at a pitch (0.05 in) (Fig. 2) and coupling interposer 100 to the PLCC (Figs. 2 and 3; p.3: paragraph [0028]), and interposer 100 further has a second plurality of contacts 106 spaced at said pitch (0.05 in) (Fig. 2) to couple the interposer 100 to the parent PWB (Figs. 2 and 3; p.3: paragraphs [0029]).

As to Claim 2, Olzak et al. further discloses that interposer 100 comprises a first surface 102a, a second surface 102b, and a plurality of conductive paths 108 between the first surface 102a and second surface 102b (Fig. 2; p.3: paragraph [0030]).

As to Claim 3, Olzak et al. further discloses interposer 100 has an edge perpendicular to first and second surfaces 102a and 102b, and wherein each of the conductive paths 108 comprises a conductive coating formed in a recessed channel in the edge (Fig. 2; p.3: paragraph [0031]).

As to Claim 50, Olzak et al. further discloses that interposer 100 is to be fixedly coupled to the parent PWB (p.3: paragraph [0032]).

As to Claim 6, Olzak et al. discloses an interposer 100, comprising a circuit board substrate 102, to couple a microelectronic device package to a circuit board (Figs. 2 and 3; p.3: paragraphs [0028] and [0032]).

As to Claim 7, Olzak et al. further discloses circuit board substrate 102 has a first surface 102a and a second surface 102b parallel to first surface 102a, interposer 100 further comprising: a first plurality of electrical contacts 104 on first surface 102a (Fig. 2; p.3: paragraph [0028]); a second plurality of electrical contacts 106 on second surface 102b (Fig. 2; p.3: paragraph [0029]); a plurality of conductive paths (each path comprising conductive elements 110 and 108), each from one of the first plurality of electrical contacts 104 to one of the second plurality of electrical contacts 106 (Fig. 3; p.3: paragraph [0030]).

As to Claim 8, Olzak et al. further discloses circuit board substrate 102 further has an edge perpendicular to the first and second surfaces 102a and 102b, wherein each of the conductive paths comprises a conductive coating formed in a recessed channel 108 in the edge (Fig. 2; p.3: paragraph [0031]).

As to Claim 10, Olzak et al. further discloses an interposer 100 comprising: a circuit board substrate 102 having a first surface 102a and a second surface 102b (Fig. 2; p.3: paragraph [0028]); a first plurality of conductive contacts 104 spaced at a pitch (0.05 in) on the first surface 102a to be fixedly coupled to an electronic component package (PLCC) (Fig. 3; p.3: paragraph [0028]); a second plurality of conductive contacts spaced at said pitch (0.05 in) on the second surface 102b (Fig. 2) to be fixedly coupled to a circuit board (i.e., a parent PWB) (Fig. 3; p.3: paragraph [0029]); a plurality of conductive paths (each path comprising conductive elements 110 and 108), each separately connecting one of the first plurality of conductive contacts 104 with one of the second plurality 106 of conductive contacts (Fig. 2; p.3: paragraph [0030]).

As to Claim 12, Olzak et al. further discloses each of the conductive paths comprises a conductive coating formed in recessed channel 108 in an edge of the substrate 102, the edge perpendicular to the first and second surfaces 102a and 102b (Fig. 2; p.3: paragraphs [0030] and [0031]).

As to Claim 13, Olzak et al. further discloses that each of the recessed channels 108 is a portion of a cylindrical through hole (Fig. 2; p.3: paragraph [0031]).

As to Claim 18, Olzak et al. discloses a die (hidden by the PLCC encapsulation) having a plurality of circuits formed thereon (p.1: paragraph [0007]) and a package substrate (the carrier element of the PLCC) having a first surface coupled to the die and a second surface (Fig. 3; p.1: paragraph [0007]); a circuit board (the parent PWB in Fig. 3); and an interposer 100 coupled between the second surface of the package (PLCC) substrate and the parent PWB, the interposer comprising: a circuit board substrate 102

having a first surface 102a and a second surface 102b (Fig. 2; p.3: paragraph [0028]); a first plurality of conductive contacts 104 disposed at a pitch (0.05 in) on the first surface 102a of circuit board substrate 102 (Fig. 3; p.3: paragraph [0028]), to be fixedly coupled to an electronic component package (i.e., a PLCC), a second plurality of conductive contacts 106 disposed at said pitch (0.05 in) on the second surface 102b of circuit board substrate 102, to be coupled to the parent PWB (Fig. 3; p.3: paragraph [0029]), and a plurality of conductive paths (each path comprising conductive elements 110 and 108), each separately connecting one of the first plurality of conductive contacts 104 with one of the second plurality of conductive contacts 106 (Fig. 3; p.3: paragraph [0030]).

As to Claim 19, Olzak et al. further discloses each of the conductive paths comprises a conductive coating formed in a recessed channel 108 in an edge of circuit board substrate 102, the edge perpendicular to the first and second surfaces 102a and 102b (Fig. 2; p.3: paragraph [0031]).

As to Claim 20, Olzak et al. further discloses each of the recessed channels 108 is a portion of a cylindrical through hole (Fig. 2; p.3: paragraph [0031]).

As to Claim 23, Olzak et al. discloses fixedly coupling a plurality of electrical contacts 104 on a first surface 102a of an interposer 102 to the electronic circuit package (PLCC) (Fig. 3; p.3: paragraph [0028]), the interposer 102 formed from a circuit board substrate having the first surface 102a, a second surface 102b (p.3: paragraph [0028]), and a plurality of conductive paths (each comprising conductive elements 110 and 108) from the first surface 102a to the second surface 102b (Figs. 2 and 3; p.3: paragraph [0030]); fixedly coupling a plurality of electrical contacts 106 on the second

surface 102b to the parent PWB, the interposer 100 wired such that the first plurality of electrical contacts 104 and the second plurality of electrical contacts 106 are spaced at an equal pitch (0.05 in) (Figs. 2 and 3; p.3: paragraphs [0028] and [0029]).

As to Claim 24, Olzak et al. further discloses the electronic circuit package includes a semiconductor die (p.1: paragraphs [0003] and [0007]).

As to Claim 25, Olzak et al. further discloses the circuit board is a motherboard (i.e., the "parent" PWB in Fig. 3).

As to Claim 26, Olzak et al. discloses a circuit board substrate member 102 having a first surface 102a and a second surface 102b parallel to each other, substrate 102 further having an edge perpendicular to the first and second surfaces 102a and 102b (Fig. 2); a first plurality of conductive contact pads 104 on first surface 102a (Fig. 2; p.3: paragraph [0028]); a second plurality of conductive contact pads 106 on the second surface (Fig. 2; p.3: paragraph [0028]); and a plurality of recessed channels 108 in the edge of the substrate member 102, extending from the first surface 102a to the second surface 102b (Fig. 2), each of the recessed channels 108 having a conductive material therein to form a conductive path between one of the first plurality of contact pads 104 and one of the second plurality of contact pads 106 (Fig. 2; p.3: paragraphs [0030] and [0031]).

As to Claim 27, Olzak et al. further discloses the recessed channels 108 are concave (Fig. 2; p.3: paragraph [0031]).

As to Claim 28, Olzak et al. further discloses each of the recessed channels is a portion of a through hole (Fig. 2; p.3: paragraph [0031]).

As to Claim 51, Olzak et al. further discloses the first plurality of conductive contact pads 104 and the second plurality of conductive contact pads are spaced at an equal pitch (0.05 in) (Fig. 2; p.3: paragraphs [0028] and [0029]).

14. Claims 10, 16 and 40-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Higashiguchi et al.

As to Claim 10, Higashiguchi et al. discloses, in Figs. 3 and 5, an interposer comprising: a circuit board substrate 30 (col.5: 58-63) having a first (upper) surface and a second (lower) surface parallel to each other; a first plurality of conductive contact pads 54 spaced at a pitch on the first (upper) surface (Figs. 7C and 7D; col.6: 40-42); a second plurality of conductive contact pads 46 or 54 spaced at said pitch on the second (bottom) surface (Figs. 5, 7C and 7D; col.5: 58-63; col.6: 40-42); and a plurality of conductive paths (plated through-holes 40), each separately connecting one of the first plurality of conductive contacts 54 with one of the second plurality of contacts 46 or 54 (Figs. 5 and 7C).

As to Claim 16, Higashiguchi et al. further discloses each of the conductive paths 40 comprises a solid conductive (copper) column 56 through the substrate 30 (Fig. 7D; col.6: 42-44) from the first surface to the second surface (Figs. 5 and 7D; col.6: 42-44).

As to Claim 40, Higashiguchi et al. discloses, in Figs. 3 and 5, an interposer comprising: a circuit board substrate 30 (col.5: 58-63) having a first (upper) surface and a second (lower) surface parallel to each other; a first plurality of conductive contact pads 54 on the first (upper) surface (Figs. 7C and 7D; col.6: 40-42); a second plurality of conductive contact pads 46 or 54 on the second (bottom) surface (Figs. 5, 7C and 7D;

col.5: 58-63; col.6: 40-42); and a plurality of solid conductive (copper) columns 56 through the substrate 30 (Fig. 7D; col.6: 42-44) perpendicular to the first and second surfaces, each in electrical contact with one of the first plurality of contact pads 54 (on the first, upper surface) and one of the second plurality of contact pads 46 or 54 (on the second, lower surface) (Figs. 5 and Fig. 7D; col.6: 42-44).

As to Claims 41 and 42, Higashiguchi et al. further discloses, in Figs. 3, 5 and 7D, a first plurality of grooves 44 in the first surface between the conductive columns 56 on the first surface and a second plurality of grooves 44 in the second surface between the conductive columns on the second surface (col.6: 3-11).

Allowable Subject Matter

15. Claims 4-5, 9, 14-15, 17, 21-22, 29-30, 31-32 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to Claims 4-5, patentability resides in the limitation wherein *each of the conductive paths comprises a solid conductive column formed through the substrate*, in combination with the other limitations of the broadest claim, Claim 4.

As to Claim 9, patentability resides in the limitation wherein *each of the conductive paths comprises a solid conductive column formed through the circuit board substrate*, in combination with the other limitations of claim.

As to Claims 14-15, patentability resides in *the device comprising a plurality of interposers coupled to each other, each being an interposer as recited in Claim 13*, in combination with the other limitations of the broadest claim, Claim 14.

As to Claim 17, patentability resides in the limitation wherein *each of the conductive columns is an alloy of Sn and Pb, comprising at least 81% Pb*, in combination with the other limitations of the claim.

As to Claims 21-22, patentability resides in the limitation wherein *each of the conductive paths comprises a solid conductive column formed through the circuit board substrate from the first surface to the second surface*, in combination with the other limitations of the broadest claim, Claim 21.

As to Claims 29-30, patentability resides in *a first plurality of grooves in the first surface between the contact pads on the first surface*, in combination with the other limitations of the broadest claim, Claim 29.

As to Claims 31-32, patentability resides in *the device comprising a plurality of interposers coupled to each other, each being an interposer as recited in Claim 26*, in combination with the other limitations of the broadest claim, Claim 31.

As to Claim 43, patentability resides in the limitation wherein *each of the conductive columns is an alloy of Sn and Pb, comprising at least 81% Pb*, in combination with the other limitations of the claim.

16. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
April 7, 2003